What is claimed is:

1. A semiconductor device, comprising:

a semiconductor chip having an electrode pad provided on a main surface thereof;

a wiring portion which is electrically connected to said electrode pad and which includes a bump portion substantially orthogonal to said main surface;

a wiring layer which is electrically connected to said wiring portion; and

a sealing layer which covers the perimeter and main surface of said semiconductor chip such that the surface of said wiring layer is exposed,

wherein said wiring layer is provided in the surface of said sealing layer, and extends from a first region of said sealing layer over said main surface to second region of said sealing layer outside the first region.

2. The semiconductor device according to claim 1, further comprising an external terminal which is provided in the second region and which is electrically connected to a portion of said wiring layer in the second region.

3. The semiconductor device according to claim 1, further comprising a conductive portion formed in a through hole provided in said sealing layer and having one and the other ends thereof, said one end of the conductive portion being electrically connected to said wiring layer.

4. The semiconductor device according to claim 2, further comprising a conductive portion formed in a through hole

provided in said sealing layer and having one end and the other ends thereof, said one end of the conductive portion being electrically connected to said wiring layer.

5. The semiconductor device according to claim 3, wherein another semiconductor device which is electrically connected to the other end of said conductive portion is stacked at said other end.

6. The semiconductor device according to claim 4, wherein another semiconductor device which is electrically connected to the other end of said conductive portion is stacked at said other end.

7. The semiconductor device according to claim 3, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

8. The semiconductor device according to claim 4, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

9. The semiconductor device according to claim 5, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

10. The semiconductor device according to claim 6, further

comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

11. A semiconductor device, comprising:

a semiconductor chip having first and second electrode pads provided on a main surface thereof;

a first wiring portion which is electrically connected to said first electrode pad and which includes a first bump portion substantially orthogonal to said main surface;

a second wiring portion which is electrically connected to said second electrode pad and which includes a second bump portion substantially orthogonal to said main surface;

a first wiring layer which is electrically connected to said first wiring portion;

a first conductive portion which is electrically connected to said second wiring portion; and

a sealing layer that covers the perimeter and main surface of said semiconductor chip such that the surfaces of said first wiring layer and first conductive portion are exposed,

wherein said first wiring layer is provided in the surface of said sealing layer, and extends from a first region of said sealing layer over said main surface to a second region of said sealing layer outside the first region; and

said first conductive portion is provided in the surface of said sealing layer within said first region.

12. The semiconductor device according to claim 11, further

comprising:

a first external terminal which is provided in said second region and which is electrically connected to a part of said first wiring layer ; and

a second external terminal which is provided in said first region and which is electrically connected to said first conductive portion,

wherein the distance between the adjoining first external terminals is greater than the distance between the adjoining second external terminals.

13. The semiconductor device according to claim 12, wherein the diameter of said first external terminal is greater than the diameter of said second external terminal.

14. The semiconductor device according to claim 11, further comprising a conductive portion formed in a through hole provided in said sealing layer and having one and the other ends thereof, said one end of the conductive portion being electrically connected to said first wiring layer.

15. The semiconductor device according to claim 12, further comprising a conductive portion formed in a through hole provided in said sealing layer and having one and the other ends thereof, said one end of the conductive portion being electrically connected to said wiring layer.

16. The semiconductor device according to claim 13, further comprising a conductive portion formed in a through hole provided in said sealing layer and having one and the other ends thereof, said one end of the conductive portion being

electrically connected to said wiring layer.

17. The semiconductor device according to claim 11, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

18. The semiconductor device according to claim 12, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

19. The semiconductor device according to claim 13, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

20. The semiconductor device according to claim 14, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

21. The semiconductor device according to claim 15, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

22. The semiconductor device according to claim 16, further

comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

23. A semiconductor device comprising:

a semiconductor chip having a main surface, on which an electrode pad is formed, and said surfaces;

a first wiring structure electrically connected to the electrode pad and including bump portion;

a second wiring structure electrically connected to the first wiring structure; and

a sealing layer which covers the main surface and the side surfaces of the semiconductor chip so that a portion of the surface of the second wiring structure is not covered with the sealing layer,

wherein the second wiring structure extends from a first region to a second region, the first region being located at the sealing layer over the main surface of the semiconductor chip and the second region being positioned at the sealing layer formed on the side surfaces of the semiconductor chip.

24. The semiconductor device according to claim 23, further comprising an external terminal which is provided in the second region and which is electrically connected to a portion of said second wiring structure.

25. The semiconductor device according to claim 23, further comprising a conductive portion formed in a through hole provided in said sealing layer and having one and the other ends

thereof, said other end of the conductive portion being electrically connected to said second wiring layer.

26. The semiconductor device according to claim 24, further comprising a conductive portion formed in a through hole provided in said sealing layer and having one and the other ends thereof, said other end of the conductive portion being electrically connected to said second wiring layer.

27. The semiconductor device according to claim 23, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

28. The semiconductor device according to claim 24, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

29. The semiconductor device according to claim 25, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.

30. The semiconductor device according to claim 26, further comprising a conductive layer formed on the reverse side of said semiconductor chip which is opposite to said main surface, wherein said conductive layer is electrically connected to the other end of said conductive portion.